ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 11, November 2014

Low Power and High Speed CMOS Circuits

T.Sheela[1], T.Muthumanickam[2], G.Ramachandran[3], A.Nagappan[4]

Research Scholar, VMRF Deemed University, Salem, India[1]
HoD/ECE, V.M.K.V.Engineering College, Salem, India[2]
AP/ECE, V.M.K.V.Engineering College, Salem, India[3]
Principal, V.M.K.V.Engineering College, Salem, India[4]

Abstract: In recent trends, multi-threshold CMOS technology is advancing to enhance performance of any digital circuits. By use of this technology any digital circuit makes use of both low threshold voltage (VDDL) and high threshold voltage (VDDH) MOSFETs. Propagation delay time of a circuit is reduced by using VDDL and consumption of power is reduced by using VDDH. One of the best techniques to reduce the power consumption is scaling the supply voltage VDD. In order to maintain the generational speed enhancement, the device threshold voltage VTH must also scale down with VDD. This paper proposes a low-power circuit with MTCMOS technology, simulation results shows that power consumption is reduced approximately by61.7%.

Keywords: Multi-threshold CMOS (MTCMOS), low power circuit, VDDH, VDDL.

I. INTRODUCTION

In the static multi-VTH technique gates in the critical paths are designed to operate at a high-VTH in order to reduce leakage power without compromising the performance. Failure due to electro migration results in high power dissipation which directly degrades the reliability of the chip. In advancement in fabrication technology, which causes integration of more transistors in an integrated circuit, chip shrinkage becomes mandatory. As a result, the magnitude of power per unit area is growing and the accompanying problem of heat removal and cooling is worsening. To maintain the chip temperature at an acceptable level the dissipated heat must be removed effectively, the cost of heat removal and cooling becomes a significant factor in these circuits.

II. POWER DISSIPATION SOURCES

In digital complementary metal-oxide-semiconductor (CMOS) circuits [1, 2, 3] there are three sources of power dissipation namely, the dynamic power dissipation, the short-circuit power dissipation and the leakage power dissipation. The average dynamic power dissipation of the CMOS logic gate, can be calculated from the energy required to charge down the total output load capacitance to ground level and charge up the output node to VDD driven by a periodic input voltage waveform with ideally zero rise- and fall-times.

$$\mathbf{P_{dynamic} = \alpha \, . \, C_{load} \, . \, V_{DD}{}^2 \, . \, f_{CLK}}$$

Where f_{CLK} is the operating frequency, C_{load} is the equivalent capacitance of the circuit; V_{DD} is the power-supply voltage and α is the activity factor that indicates how often the circuit switches with respect to the operating frequency.

A signal of finite rise and fall time applied to the input of a CMOS circuit causes the short-circuit power dissipation. Both the NMOS and the PMOS transistors conduct simultaneously for a short duration due to the finite rise and fall time of the input signal, forming the direct current path between the power-supply and ground.

For a symmetric CMOS inverter with very small capacitive load,
$V_{Tn} = V_{Tp} = V_T$ and
$k_n = k_p = k$ and the input is driven with a waveform with $\tau_{rise} = \tau_{fall} = \tau$.

$$\mathbf{P_{(short\text{-}circuit)} = 1/12.k.\tau. \, f_{CLK}. \, (V_{DD}\text{-}2VT)^3}$$

The short-circuit power dissipation depends on the rise and fall time of the input signal. The two components of leakage current in CMOS circuit are reverse leakage current and sub-threshold leakage current is illustrated in fig.1 and fig.2 respectively. When the P-N junction between the drain and the bulk of the transistor is reversely biased the reverse diode leakage occurs. The reverse leakage current of the P-N junction is shown in the figures.

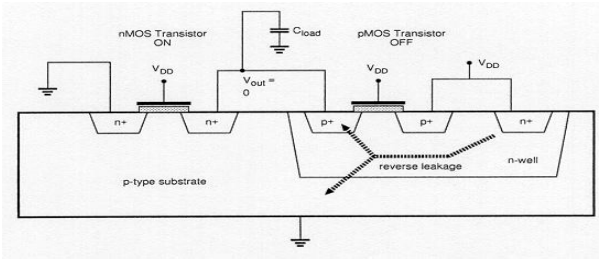

Fig.1 Reverse leakage current path in a CMOS inverter with high input voltage

Another component of leakage current is sub-threshold leakage current [4,5,6], which occurs due to carrier diffusion between the drain and source regions of the transistor in weak inversion.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 11, November 2014

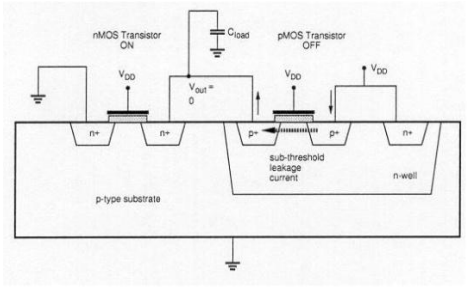

Fig.2 Subthreshold leakage current path in a CMOS inverter with high input voltage

III. HIGH SPEED AND LOW-POWER MULTI-THRESHOLD VOLTAGE LEVEL CONVERTER

In the static multi-VTH technique [9, 10], gates in the critical paths are designed to operate at a high-VTH in order to reduce leakage power without compromising the performance; similarly the gates are operated at a low-VTH to maintain high performance. However in aggressive high-performance low-power circuit topologies that have several balanced critical paths, many gates cannot be slow down, hence a merger leakage reduction can be achieved.

It is a known fact that some CMOS circuits [7, 8] operate at lower supply voltages (VDDL) while other at high supply voltages (VDDH). In order to overcome static current during circuit operation level converters between the VDDL and VDDH CMOS circuits.

Several multi-threshold (Multi-VTH) level converter circuits [1,2 3] are proposed and it is compared with the conventional circuits for operating at different supply voltages (Multi-VDD).Unlike the previously published level converters that rely on feedback, the proposed level converters employ a multi-VTH CMOS technology [7, 8] in order to eliminate the static dc current. The high threshold voltage pull-up network transistors in the new level converters are directly driven by the low-swing signals without producing a static dc current problem.

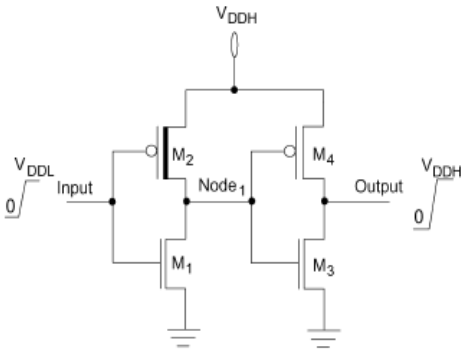

Figure.1 Multi-VTH based level converter

Tabulation I: Power consumed by the converters with Multi –VTH

VDDL	VDDH	Average propagation delay (ps)	Power in µ watts
0.5V	1.8V	**1030**	*3.08*
1V	1.8V	**165**	*2.11*
1.2V	1.8V	**137**	*2.15*

After analyses of this level converter it is identified as the efficient level converter with high processing speed and low power utilization. This level converter does not use feedback path and also suppresses dc current path driven by low voltage-swing input signals.

IV. CONCLUSION

The level converter offers a significant power saving and speed enhancement to the several applications including LFSR counter, by eliminating the static dc current and charge leakage existing in the CMOS circuits. The dc current paths in CMOS gates driven by low swing input signals are suppressed, as the circuit does not use any feedback path. When the circuit is optimized for power consumption in 0.18μ TSMC CMOS technology, it showed significant power saving with improved speed.

REFERENCES

[1] T Muthumanickam, A Nagappan, T Sheela "*Analysis Of High Performance VLSI For Telecommunication Data*", IRACST-Engineering Science and technology: An International journal (ESTIJ), ISSN: 2250-3498, pp 138-14,Vol.2,No.1, 2012.

[2] T Sheela, T Muthumanickam, A Nagappan "*Design of High-Speed Low-Power Two Level Voltage Converters using Multi-VTH CMOS Technology*" International Journal of Computer Applications,ISSN: 0975-8887, pp- 49-52,Vol 84, No-14, 2013.

[3] Mutoh S et al, "*1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS*", pp. 847-854, August 1995

[4] Neil H. E. Weste and K. Eshraghian, Principle of CMOS VLSIDesign, 2nd Ed.addison Wesley, 1993.

[5] G.Ramachandran, T.Sheela "*Low power modeling of CMOS inverter and D-Flip flop*" Journal of Computer Information Systems 6 (5), 39-57,2013

[6] G.Ramachandran, N.Manikanda Devarajan, T.Muthumanickam, et al, "*Comparative study and implementation mixed level & mixed signal simulation using PSpice and VHDL*",IJCER,pp-218-228,ISSN:2250-3005, vol 2,issue 8, 2012

[7] T Sheela, T Muthumanickam et al "*A LFSR based Binary Numeral System Using CMOS VLSI*" International Journal of VLSI and Embedded Systems-IJVES ISSN:2249-6556, Vol 3, Issue 4,2012.

[8] T Muthumanickam, A Nagappan, T Sheela" *Performance Analysis Of Cryptographic Vlsi Data*" IRACST–International Journal of Computer Networks and Wireless communication, pp 91-97, 2012

[9] Sheriff A. Tawfik and Volkan Kursun , "*Low power and high speed Multi threshold voltage Interface Circuit*" IEEE Trans ,VLSI Systems, MAY 2009, Vol.17 NO 5.

[10] Jongyoon Jung; Taewhan Kim, "*Statistical Viability Analysis for Detecting False Paths Under Delay Variation*," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Jan. 2013 Vol.32, no.1, pp.111-123.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 11, November 2014

BIOGRAPHIES

Ms T.SHEELA obtained her Master degree from Anna University in 2008 and pursuing Ph.D in the area of VLSI. At present, she is an associate professor in Department of Electronics and Communication Engineering in VMKVEC, Salem. She is a member of IEEE and IEEE-AESS, and also a Life member of ISTE. She has published many papers in National and International Conferences and Journals. Her research interests include VLSI circuits, Digital circuit, Electronic circuits and optical communication.

Mr. T.MUTHUMANICKAM obtained his M.Tech degree from SASTRA University in 2002 and obtained his Ph.D in 2013 in the area of VLSI. At present, he is a professor and head in Department of Electronics and Communication Engineering in VMKVEC, Salem. He is a member of IEEE and IEEE-AESS, and also a Life member of ISTE and IETE. He has published many papers in International Conferences and Journals. His research interests include VLSI circuits, and digital signal processing.

Mr. G. Ramachandran obtained his M.Tech degree from SRM University (Chennai) in 2009. At present, he is an Assistant Professor in Department of Electronics and Communication Engineering at VMKVEC, Salem. He is a Life member of ISTE. He has published many numbers of papers in National and International Conferences and Journals. His research interests include digital signal processing, DSP processors, computer vision and image understanding, modelling with hardware description languages VHDL and VERILOG, Digital circuits and undergoing research in embedded microprocessor systems and VLSI digital chip design.

Mr. A.Nagappan obtained his M.S degree from BITS Pilani University and Ph.D. in Computer Science and Engineering. At present, he is the principal of VMKVEC, Salem. He is a member of IEEE and IEEE-AESS, and also a Life member of ISTE, IE, etc. He has vast teaching experience and his research area includes in the field of Mammography, Wavelet Transform, Medical Imaging. He has published many papers in International Conferences and Journals.